[EXP 1-CMOS Inverter Design - GIT HUB](https://lms2.ece.saveetha.in/mod/url/view.php?id=374)

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**Ex No: 01 - Design & Implementation of CMOS Inverter Design Using Cadence EDA Tools**

**Aim:**

The aim is to create and simulate a CMOS inverter circuit with Cadence EDA tools, assess its key electrical properties, and explore foundational CMOS principles, including the design workflow and simulation approaches.

**Tools Required:**

**Cadence EDA Suite**

* **Virtuoso Schematic Editor** (for circuit design)
* **Spectre Simulator** (for circuit simulation)

**Process Design Kit (PDK)**

* CMOS technology library (e.g., 180nm, 45nm node)

**Computer System**

* Minimum **4GB RAM** and a **multi-core processor**

**Procedure:**

**1. Launch Cadence Virtuoso Environment:**

Open the Cadence Virtuoso tool and set up the working library.

Create a new schematic cell view for the CMOS Inverter design.

**2. Schematic Design:**

Select the NMOS and PMOS transistors from the library.

Connect the NMOS transistor with its source terminal to GND and its drain terminal to the output node.

Connect the PMOS transistor with its source terminal to VDD and its drain terminal to the same output node as NMOS.

Join the gate terminals of both transistors to form the input node.

Connect input voltage sources Vdc and Vpulse

**3. Simulation:**

Check the Design for Errors and proceed for Simulation

Launch the Analog Design Environment (ADE).

Configure transient analysis for time-domain response.

Set the simulation parameters such as voltage sweep range and step size.

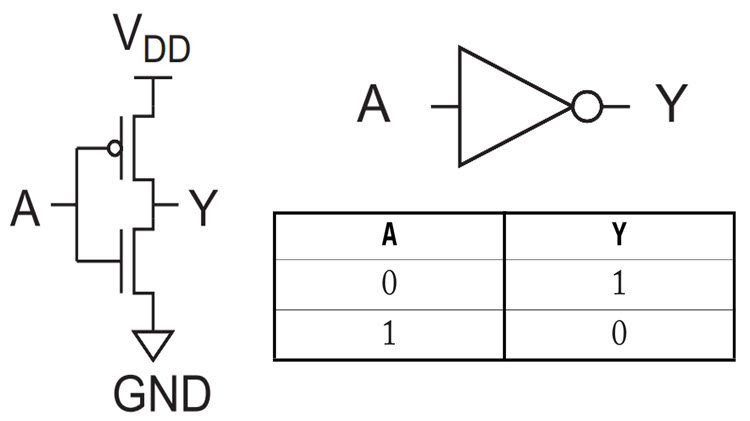
Use Spectre simulator to perform transient and DC analyses.

**4. Waveform Analysis:**

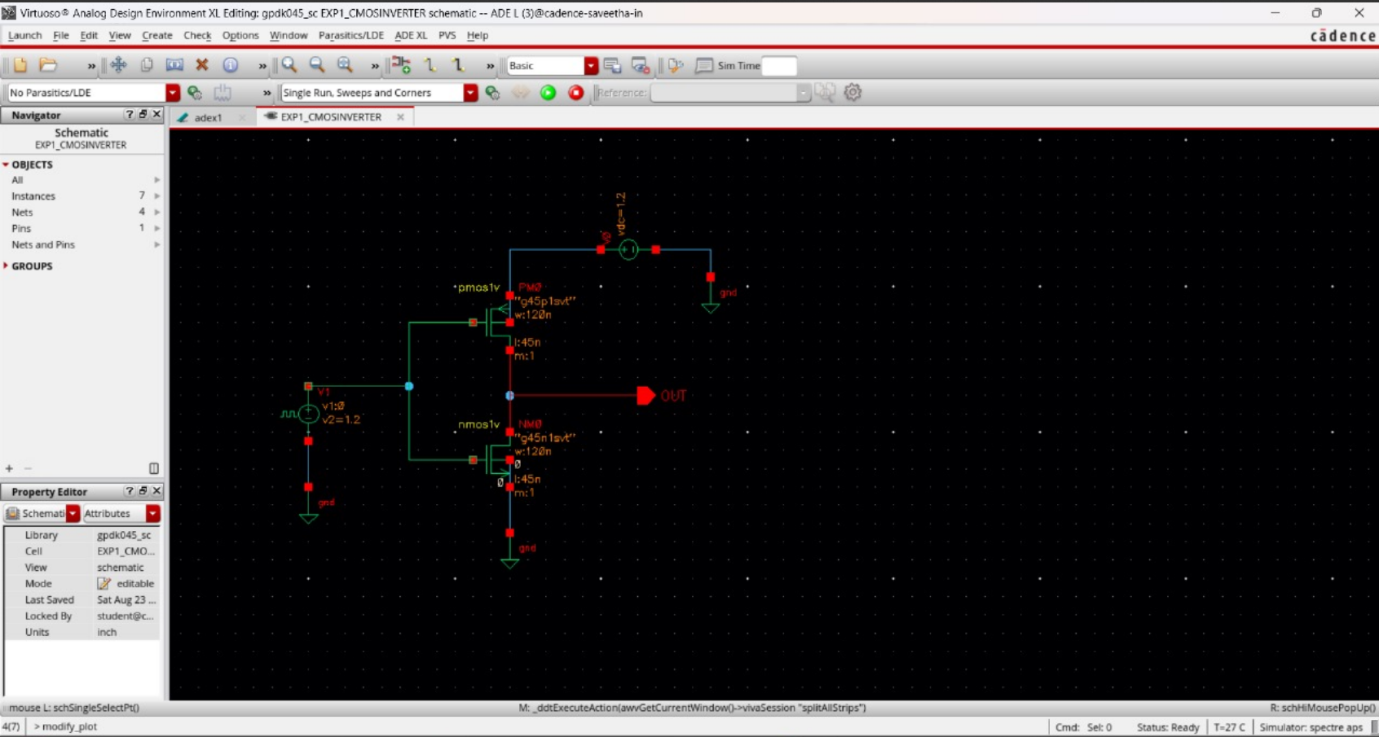
Observe the output voltage waveform concerning the input voltage.

**Circuit Diagram:**

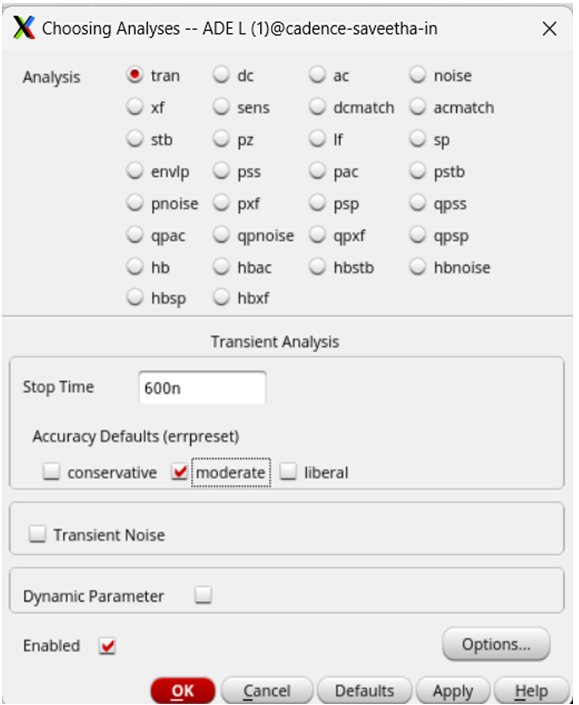
**1. CMOS Inverter:**

[](https://private-user-images.githubusercontent.com/157122075/427961687-e3e06487-52b2-4b56-9dcd-03c5c9394a4c.png?jwt=eyJ0eXAiOiJKV1QiLCJhbGciOiJIUzI1NiJ9.eyJpc3MiOiJnaXRodWIuY29tIiwiYXVkIjoicmF3LmdpdGh1YnVzZXJjb250ZW50LmNvbSIsImtleSI6ImtleTUiLCJleHAiOjE3NTY0ODQ0MDUsIm5iZiI6MTc1NjQ4NDEwNSwicGF0aCI6Ii8xNTcxMjIwNzUvNDI3OTYxNjg3LWUzZTA2NDg3LTUyYjItNGI1Ni05ZGNkLTAzYzVjOTM5NGE0Yy5wbmc_WC1BbXotQWxnb3JpdGhtPUFXUzQtSE1BQy1TSEEyNTYmWC1BbXotQ3JlZGVudGlhbD1BS0lBVkNPRFlMU0E1M1BRSzRaQSUyRjIwMjUwODI5JTJGdXMtZWFzdC0xJTJGczMlMkZhd3M0X3JlcXVlc3QmWC1BbXotRGF0ZT0yMDI1MDgyOVQxNjE1MDVaJlgtQW16LUV4cGlyZXM9MzAwJlgtQW16LVNpZ25hdHVyZT0xZTYyNTA1OWU4ODI3NjE0ZTQ2MWYzYTVlMTUxOGI3Mjg3ODMwNmM2YjdlZTEzYWYwZDc2NDM1NzNkNWY5YTE5JlgtQW16LVNpZ25lZEhlYWRlcnM9aG9zdCJ9.H6OssADgdon7bwjNxGP7_oHeaNFxZo9Tkf-itkTfHw4)

**2. Schematic of CMOS Inverter:**

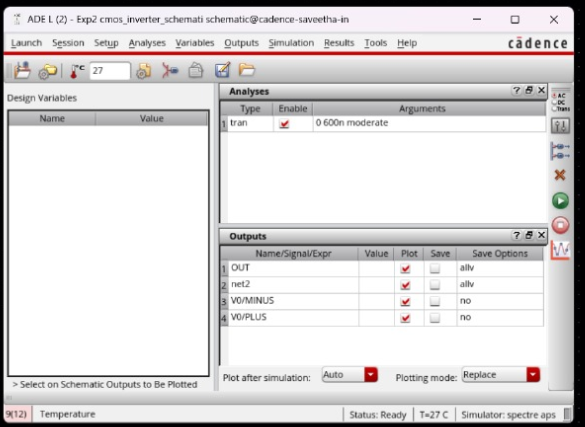


**3. Transient Response Setup:**

[](https://private-user-images.githubusercontent.com/157122075/427962432-ecdf8ecc-5dfe-404d-ba08-85b1982881cf.png?jwt=eyJ0eXAiOiJKV1QiLCJhbGciOiJIUzI1NiJ9.eyJpc3MiOiJnaXRodWIuY29tIiwiYXVkIjoicmF3LmdpdGh1YnVzZXJjb250ZW50LmNvbSIsImtleSI6ImtleTUiLCJleHAiOjE3NTY0ODQ0MDUsIm5iZiI6MTc1NjQ4NDEwNSwicGF0aCI6Ii8xNTcxMjIwNzUvNDI3OTYyNDMyLWVjZGY4ZWNjLTVkZmUtNDA0ZC1iYTA4LTg1YjE5ODI4ODFjZi5wbmc_WC1BbXotQWxnb3JpdGhtPUFXUzQtSE1BQy1TSEEyNTYmWC1BbXotQ3JlZGVudGlhbD1BS0lBVkNPRFlMU0E1M1BRSzRaQSUyRjIwMjUwODI5JTJGdXMtZWFzdC0xJTJGczMlMkZhd3M0X3JlcXVlc3QmWC1BbXotRGF0ZT0yMDI1MDgyOVQxNjE1MDVaJlgtQW16LUV4cGlyZXM9MzAwJlgtQW16LVNpZ25hdHVyZT1hYzkyNzgwODMwN2I5MTMyNzk4ZjQ0NjQ3MmZjNDEwOGIyNTI2OGU4YTc3NjY3NWU0MjExMTBkYzFlZmNlODMyJlgtQW16LVNpZ25lZEhlYWRlcnM9aG9zdCJ9.7DJ2zeRafBBFOJ2VaON7qeqsmFtC_UMqMu7iNQ1vsvk)

A screenshot of a computer

AI-generated content may be incorrect.

[](https://private-user-images.githubusercontent.com/157122075/427962928-2611bd19-13be-4413-a662-9de3b555981d.png?jwt=eyJ0eXAiOiJKV1QiLCJhbGciOiJIUzI1NiJ9.eyJpc3MiOiJnaXRodWIuY29tIiwiYXVkIjoicmF3LmdpdGh1YnVzZXJjb250ZW50LmNvbSIsImtleSI6ImtleTUiLCJleHAiOjE3NTY0ODQ0MDUsIm5iZiI6MTc1NjQ4NDEwNSwicGF0aCI6Ii8xNTcxMjIwNzUvNDI3OTYyOTI4LTI2MTFiZDE5LTEzYmUtNDQxMy1hNjYyLTlkZTNiNTU1OTgxZC5wbmc_WC1BbXotQWxnb3JpdGhtPUFXUzQtSE1BQy1TSEEyNTYmWC1BbXotQ3JlZGVudGlhbD1BS0lBVkNPRFlMU0E1M1BRSzRaQSUyRjIwMjUwODI5JTJGdXMtZWFzdC0xJTJGczMlMkZhd3M0X3JlcXVlc3QmWC1BbXotRGF0ZT0yMDI1MDgyOVQxNjE1MDVaJlgtQW16LUV4cGlyZXM9MzAwJlgtQW16LVNpZ25hdHVyZT1lOWFmNTY2MDUyYjUxNWM1YzdmZTNiNDk3MTJiZTcxZWEyMDExODY4ZTQ2NWQxMDUxNTFmZDE2ODIyNWY5OTI3JlgtQW16LVNpZ25lZEhlYWRlcnM9aG9zdCJ9.lZvY1f5q6KHhhB3Ea5Nfxqb_pHZ_q6ENY60O-FDwM0E)

A computer screen shot of a computer program

AI-generated content may be incorrect.

**Output**

**1.Transient Analysis Output**

A screenshot of a computer

AI-generated content may be incorrect.

**Results:**

1. Successfully designed the CMOS inverter schematic using Cadence EDA tools.
2. The simulation results demonstrated the correct logic operation of the inverter, where the output voltage switches between high (Vdd) and low (0V) levels, corresponding to the input voltage transitions.
3. The Voltage Transfer Characteristic (VTC) curve was plotted, showing the relationship between input and output voltages.